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MANUFACTURE OF ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

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ABSTRACT

PURPOSE: To provide the manufacture of the active matrix type liquid crystal display device which excellently protects its internal TFTs against static electricity and effective prevents their dielectric breakdown and characteristic deterioration.

CONSTITUTION: A short-circuit line 9 which short-circuits scanning wirings 2 and signal wirings 4 is arranged on the edge part of one glass substrate 1. Liquid crystal is charged between an array substrate 10 and an opposite substrate and then the peripheral edge part of the glass substrate is cut into a specific product shape so that the short circuit line 9 is left. Then driving ICs 11 are mounted on the edge parts of the glass substrate 1 and after the scanning wirings 2 and signal wirings 4 are connected to the driving ICs 11, the connection places of the short-circuit line 9, and the scanning wirings 2 and signal wirings 4 are disconnected.

31例3

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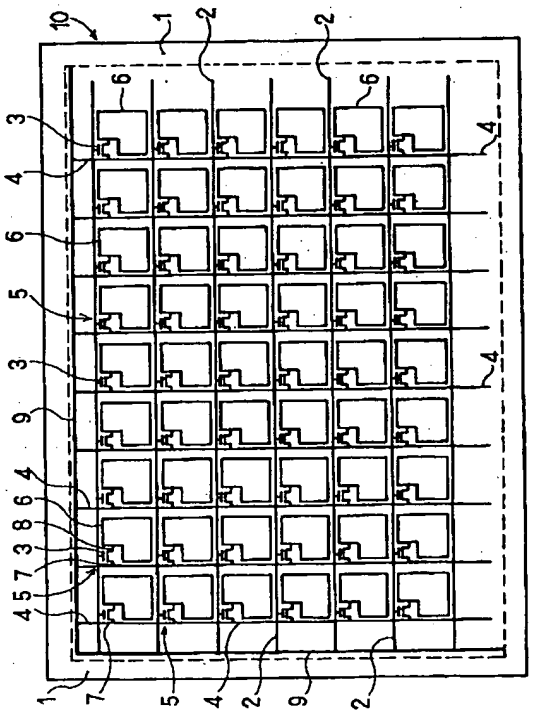
(54)【発明の名称】　アクティブマトリックス型液晶表示装置の製造方法

(57)【要約】

【目的】　内蔵されたＴＦＴを静電気から良好に保護し、その絶縁破壊や特性劣化を効果的に防止し得るアクティブマトリックス型液晶表示装置の製造方法を提供する。

【構成】　一方のガラス基板１の縁部上に走査配線２と信号配線４とを短絡させる短絡線９が配設される。アレイ基板１０と対向基板間に液晶を封入した後、ガラス基板の周縁部を所定の製品形状に短絡線９を残した状態で切断する。その後、ガラス基板１の縁部上に駆動用ＩＣ１１を実装し、走査配線２及び信号配線４を駆動用ＩＣ１１に接続した後、短絡線９と走査配線２及び信号配線４との接続箇所を切り離す。



【特許請求の範囲】

【請求項１】　一方のガラス基板上に走査配線と信号配線がマトリックス状に配設され、各配線の交差位置に薄膜トランジスタを接続してアレイ基板が形成され、他方のガラス基板上に共通電極を形成した対向基板が形成され、アレイ基板と対向基板の上面に配向膜を形成し、間隙をおいて平行に貼り合わせた該アレイ基板と該対向基板間に液晶を封入してなるアクティブマトリックス型液晶表示装置の製造方法において、

前記一方のガラス基板の縁部上に前記走査配線と前記信号配線とを短絡させる短絡線が配設され、前記アレイ基板と対向基板間に液晶を封入した後、前記ガラス基板の周縁部を所定の製品形状に該短絡線を残した状態で切断し、該ガラス基板の縁部上に駆動用集積回路を実装し、前記走査配線及び信号配線を該駆動用集積回路に接続した後、該短絡線と走査配線及び該信号配線との接続箇所を切り離すことを特徴とするアクティブマトリックス型液晶表示装置の製造方法。

【請求項２】　一方のガラス基板上に走査配線と信号配線がマトリックス状に配設され、各配線の交差位置に薄膜トランジスタを接続してアレイ基板が形成され、他方のガラス基板上に共通電極を形成した対向基板が形成され、アレイ基板と対向基板の上面に配向膜を形成し、間隙をおいて平行に貼り合わせた該アレイ基板と該対向基板間に液晶を封入してなるアクティブマトリックス型液晶表示装置の製造方法において、

前記一方のガラス基板の縁部上に各走査配線と各信号配線に対応して多数の保護用薄膜トランジスタを配設し、該保護用薄膜トランジスタの各ドレイン電極を短絡させるドレイン短絡線を該ガラス基板の縁部に沿って配設し、該保護用薄膜トランジスタの各ゲート電極を短絡させるゲート短絡線を該ガラス基板の縁部に沿って配設し、その後の製造工程中、該ドレイン短絡線を接地し、該ゲート短絡線に一定電圧を印加して該保護用薄膜トランジスタを導通状態とすることを特徴とするアクティブマトリックス型液晶表示装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、薄膜トランジスタ（以下ＴＦＴと略称する）を各画素毎に設置してスイッチング動作させ、画像を表示するアクティブマトリックス型液晶表示装置の製造方法に関する。

【０００２】

【従来の技術】この種のアクティブマトリックス型液晶表示装置は、基本的には、一方のガラス基板上に走査配線と信号配線がマトリックス状に配設され、それらの交差位置にＴＦＴ及び画素電極を設けてアレイ基板が形成され、他方のガラス基板上に共通電極を形成した対向基板が形成され、アレイ基板と対向基板の上面に配向膜を形成し、間隙をおいて平行に貼り合わせたアレイ基板と対向基板間に液晶を封入して形成される。

【０００３】このような液晶表示装置の製造工程では、一般に、製造室内の空気流、作業者の衣服の摩擦、或は配向膜のラビング処理などによって、多くの静電気が発生する。液晶表示装置に内蔵されるＴＦＴはこの種の静電気に対し非常に弱く、特に多量の静電気が発生しその電荷が走査配線や信号配線に印加された場合、各走査配線や信号配線間等で高電圧が発生し、そこに接続されたＴＦＴ内部で絶縁破壊が発生し、ＴＦＴの特性が部分的に或は全面的に劣化する問題が生じる。

【０００４】そこで、従来では、アレイ基板の製造時に、基板の周縁部上に短絡線を配設し、その短絡線に全ての走査配線と信号配線を接続し、配向膜のラビング処理時などに発生する静電気を短絡線を通して流し、ＴＦＴを保護するようにしていた。

【０００５】しかし、このようなアレイ基板の製造時に、走査配線と信号配線を短絡線に接続した状態では、製造工程中におけるＴＦＴなどの断線ショート検査、プローブ検査等が行なえないため、ラビング処理の後、或はアレイ基板と対向基板を貼り合せて液晶を封入して液晶パネルを形成した後、各走査配線と信号配線を短絡線から切り離していた。

【０００６】このため、各走査配線と信号配線を短絡線から切り離した後、駆動用ＩＣを各走査配線と信号配線に接続するまでの間、ＴＦＴは静電気から保護されない状態となり、この間の製造工程中における製品の運搬時や人体との接触により、静電気が発生した場合、上記のようなＴＦＴの絶縁破壊や特性劣化が発生する問題があった。

【０００７】

【発明が解決しようとする課題】そこで、製造時における液晶パネル内のＴＦＴの特性劣化や絶縁破壊を防止するために、従来では、アレイ基板の全面を絶縁膜により被覆してＴＦＴを保護する技術（特開昭６４－３２２３４号公報）、アレイ基板の周縁部に模擬電極を配設し、その模擬電極に静電気の電荷を集めるようにして、内側のＴＦＴを保護する技術（特開昭６４－５９３２０号公報、特開昭６４－５９３２１号公報）など各種の静電気対策が提案されている。

【０００８】しかし、これら何れの技術においても、ＴＦＴの静電気からの保護において、充分な効果をあげることができず、依然として製品の歩溜りを低下させる原因となっていた。

【０００９】本発明は、上記の課題を解決するためになされたもので、内蔵されたＴＦＴを静電気から良好に保護し、その絶縁破壊や特性劣化を効果的に防止し得るアクティブマトリックス型液晶表示装置の製造方法を提供することを目的とする。

【００１０】

【課題を解決するための手段】このために、第一発明の

製造方法は、一方のガラス基板上に走査配線と信号配線がマトリックス状に配設され、各配線の交差位置に薄膜トランジスタを接続してアレイ基板が形成され、他方のガラス基板上に共通電極を形成した対向基板が形成され、アレイ基板と対向基板の上面に配向膜を形成し、間隙をおいて平行に貼り合わせたアレイ基板と対向基板間に液晶を封入してなるアクティブマトリックス型液晶表示装置の製造方法において、一方のガラス基板の縁部上に走査配線と信号配線とを短絡させる短絡線が配設され、アレイ基板と対向基板間に液晶を封入した後、ガラス基板の周縁部を所定の製品形状に短絡線を残した状態で切断し、ガラス基板の縁部上に駆動用集積回路を実装し、走査配線及び信号配線を駆動用集積回路に接続した後、短絡線と走査配線及び信号配線との接続箇所を切り離すように構成される。

【００１１】第二発明の製造方法は、一方のガラス基板上に走査配線と信号配線がマトリックス状に配設され、各配線の交差位置に薄膜トランジスタを接続してアレイ基板が形成され、他方のガラス基板上に共通電極を形成した対向基板が形成され、アレイ基板と対向基板の上面に配向膜を形成し、間隙をおいて平行に貼り合わせた該アレイ基板と対向基板間に液晶を封入してなるアクティブマトリックス型液晶表示装置の製造方法において、一方のガラス基板の縁部上に各走査配線と各信号配線に対応して多数の保護用薄膜トランジスタを配設し、保護用薄膜トランジスタの各ドレイン電極を短絡させるドレイン短絡線をガラス基板の縁部に沿って配設し、保護用薄膜トランジスタの各ゲート電極を短絡させるゲート短絡線をガラス基板の縁部に沿って配設し、その後の製造工程中、ドレイン短絡線を接地し、ゲート短絡線に一定電圧を印加して保護用薄膜トランジスタを導通状態とするように構成される。

【００１２】

【作用・効果】第一発明の製造方法では、アクティブマトリックス型液晶表示装置の製造時、ラビング処理や液晶封入などの工程中、及びその後、ガラス基板の周縁部を製品形状に切断する工程などを含む各走査配線と各信号配線が駆動用ＩＣに接続されるまで、各走査配線と各信号配線は短絡線により短絡される。このため、そこに接続された各ＴＦＴのソース電極及びゲート電極は短絡されて同電位となり、静電気による電荷が各走査配線や信号配線に注入された場合でも、ＴＦＴのソース電極とゲート電極間に高電圧がかかることはなく、静電気によって破壊されやすいソース・ゲート間の絶縁層は確実に保護される。

【００１３】また、ガラス基板の縁部上に駆動用ＩＣを実装して走査配線及び信号配線に接続した後、短絡線と走査配線及び信号配線との接続箇所を切り離すため、従来のように、短絡線と走査配線及び信号配線が切り離されることによって、走査配線と信号配線が開放された状態となることがなく、つまり短絡線の切り離し後、駆動用ＩＣが走査配線と信号配線に接続されるまでの配線が開放されている期間がなくなり、製造工程全体にわたって、ＴＦＴを静電気から効果的に保護することができる。

【００１４】第二発明の製造方法では、アレイ基板の製造工程中、ガラス基板の縁部上に各走査配線と各信号配線に対応して多数の保護用薄膜トランジスタを配設し、保護用薄膜トランジスタの各ドレイン電極を短絡させるドレイン短絡線をガラス基板の縁部に沿って配設し、保護用薄膜トランジスタの各ゲート電極を短絡させるゲート短絡線をガラス基板の縁部に沿って配設する。そして、その後のラビング処理や液晶封入などの工程中、ドレイン短絡線を接地し、ゲート短絡線に一定電圧を印加して保護用薄膜トランジスタを導通状態とする。

【００１５】このため、各走査配線と各信号配線は、製造工程中、常時、保護用ＴＦＴとドレイン短絡線を介して接地された状態となり、各ＴＦＴのソース電極及びゲート電極が短絡されて同電位となるため、静電気による電荷が各走査配線や信号配線に注入された場合でも、ＴＦＴのソース電極とゲート電極間に高電圧がかかることはなく、静電気によって破壊されやすいソース・ゲート間の絶縁層は確実に保護される。

【００１６】

【実施例】以下、本発明の実施例を図面に基づいて説明する。

【００１７】図１～図３は、上記第一発明の実施例を示し、図１はアクティブマトリックス型液晶表示装置の製造時におけるアレイ基板１０の概略平面図を示している。

【００１８】アレイ基板１０を製造する場合、先ず、ガラス基板１上に多数の走査配線２を一定の間隔をおいて平行に形成すると共に、多数のＴＦＴ５を配置する各々の位置に、そのゲート電極３を各走査配線２に接続して形成する。この走査配線２及びゲート電極３は、クロム等の金属を用いて、スパッタリング法及びホトリソグラフィー法等により形成される。

【００１９】また、このとき、ガラス基板の縁部、例えば図１の上縁部と左縁部に、Ｌ字状の短絡線９がクロム等の金属を用いて形成され、前記各走査配線２の左端部がその短絡線９に接続される。

【００２０】次に、各ＴＦＴ５のゲート電極３上にゲート絶縁膜を形成し、ゲート絶縁膜の上に活性層とドーピング層を島状に形成する。

【００２１】次に、ゲート絶縁膜の上に、ＩＴＯ等の金属を用いて画素電極６を、スパッタリング法及びホトリソグラフィー法により形成する。そして、モリブデン、アルミニウム等の金属を用いて、多数の信号配線４を前記走査配線２と直交する方向に一定間隔をおいて平行に形成し、さらに、同様の金属及び同方法を用いて、各Ｔ

ＦＴ５のソース電極７を各信号配線４に接続して形成し、且つドレイン電極８を画素電極６に接続して形成する。これらの信号配線４は、図１に示すように、その上端が上縁位置に配設された前記短絡線９に接続される。

【００２２】このようにして、ガラス基板１上に走査配線２と信号配線４がマトリックス状に形成され、それらの交差位置にＴＦＴ５が配置されてアレイ基板１０が製造される。

【００２３】一方、アレイ基板１０と対向して配設される対向基板（図示せず）は、別のガラス基板上に、ＩＴＯ等からなる共通電極を形成して製造される。

【００２４】そして、アレイ基板１０と対向基板の表面（内側）にポリイミド等からなる配向膜を形成し、焼成した後、配向膜の表面にはラビング処理が施される。このラビングを行う際、空気やパイル等の摩擦により非常に多くの静電気が発生する。しかし、アレイ基板１０における各走査配線２と各信号配線４は、短絡線９によって短絡されているため、そこに接続された各ＴＦＴ５のソース電極７及びゲート電極３は短絡されて同電位となり、静電気による電荷が各走査配線２や信号配線４に注入された場合でも、ソース電極７とゲート電極３間に高電圧がかかることはなく、静電気によって破壊されやすいソース・ゲート間の絶縁層は確実に保護される。

【００２５】次に、アレイ基板１０と対向基板を平行に、その配向膜を対向させて一定の間隔をおいて重ね合せ、周囲をシール材（接着剤）で注入口となる部分を残してシールし、焼成した後、その注入口から基板の内部に液晶を注入し、そして、注入口を封止する。

【００２６】その後、アレイ基板１０及び対向基板のガラス基板の周縁部が、製品形状となるように所定寸法だけ切断されるが、このとき、図２のように、短絡線９はガラス基板１上に残して縁部が切断される。したがって、各走査配線２と信号配線４が短絡線９によって短絡された状態は、その後も継続され、製造工程中における作業者との接触や運搬動作等によって静電気が帯電した場合にも、ＴＦＴ５のソース電極７及びゲート電極３は短絡されて、同電位となり、上記と同様にＴＦＴ５を保護することができる。

【００２７】なお、上記では、各走査配線２と各信号配線４を、１本の短絡線９によって短絡接続しているが、各走査配線２に接続した短絡線（図の垂直部分）と各信号配線４に接続した短絡線（水平部分）を切り離し、その間に高抵抗を接続すれば、ＴＦＴ５を静電気から保護しながら、その短絡線を利用してＴＦＴ５の性能を検査することができる。

【００２８】この液晶表示装置は、駆動用ＩＣがガラス基板１上に直接実装される所謂ＣＯＧ型であり、図２に示すように、ガラス基板１の右縁部と下縁部にその駆動用ＩＣを実装するためのスペースが形成されている。

【００２９】そこで、駆動用ＩＣ１１は、図３に示すように、ガラス基板１の右縁部と下縁部のスペースに、その各端子を走査配線２及び信号配線４の延長部分に接続するように、実装される。また、短絡線９は駆動用ＩＣ１１のＧＮＤ端子に接続される。

【００３０】そして、駆動用ＩＣ１１を実装した後、図３に示すように、各走査配線２、各信号配線４と短絡線９との接続部分がレーザカッター等により切り離される。

【００３１】このように、ガラス基板１の縁部上に駆動用ＩＣ１１を実装して走査配線２及び信号配線４に接続した後、短絡線９と走査配線２及び信号配線４との接続箇所を切り離すため、従来のように、ガラス基板の縁部の切断と共に短絡線が切除される等によって、走査配線と信号配線が開放された状態となることがなく、製造工程全体にわたって、ＴＦＴ５を静電気から効果的に保護することができる。

【００３２】また、短絡線９は駆動用ＩＣ１１のＧＮＤ端子に接続された状態で製品となるため、液晶表示装置の縁部にアース接続された導線が配設され、製品の静電気保護に役立てることができる。

【００３３】図４は上記第二発明の実施例であり、製造時におけるアレイ基板２０の概略平面図を示している。

【００３４】このアレイ基板２０を製造する場合、先ず、ガラス基板２１上に多数の走査配線２２を一定の間隔をおいて形成すると共に、多数のＴＦＴ２５を配置する各々の位置に、そのゲート電極２３を各走査配線２２に接続して形成する。この走査配線２２及びゲート電極２３は、クロム等の金属を用いて、スパッタリング法及びホトリソグラフィー法等により形成される。

【００３５】同時に、ガラス基板２１の縁部、例えば図４の上縁部と右縁部に、ゲート短絡線２９をクロム等の金属で形成し、後述の保護用ＴＦＴ３０のゲート電極３３をそのゲート短絡線２９に接続して形成する。これらの保護用ＴＦＴ３０は、ガラス基板２０の上縁部と右縁部に沿って、各走査配線２２及び後述の信号配線２４に対応して配設される。

【００３６】次に、各ＴＦＴ２５のゲート電極２３及び各保護用ＴＦＴ３０のゲート電極３３上に、ゲート絶縁膜を形成し、ゲート絶縁膜の上に活性層とドーピング層を島状に形成する。

【００３７】次に、ゲート絶縁膜の上に、ＩＴＯ等の金属を用いて画素電極２６を、スパッタリング法及びホトリソグラフィー法により形成し、同時に、ガラス基板１の上縁部と右縁部に沿って、ドレイン短絡線３９を同金属、同方法により形成する。

【００３８】次に、モリブデン、アルミニウム等の金属を用いて、多数の信号配線２４を前記走査配線２２と直交する方向に一定間隔をおいて同様な方法で形成する。

【００３９】そして、同様の金属、同様な方法により、各ＴＦＴ２５のソース電極２７を各信号配線２４に接続

して形成し、且つドレイン電極２８を画素電極２６に接続して形成し、同時に、各保護用ＴＦＴ３０のドレイン電極３８をドレイン短絡線３９に接続して形成し、さらに各保護用ＴＦＴ３０のソース電極３７を各信号配線２４に接続して形成する。

【００４０】なお、保護用ＴＦＴ３０はＴＦＴ２５の形成と同時にガラス基板２１上に形成されるため、図４の右縁部に配置される保護用ＴＦＴ３０は、上縁部に配置される保護用ＴＦＴ３０を逆スタガード型とした場合、ゲート側とソース・ドレイン側をその逆に形成したスタガード型とすればよい。

【００４１】このようにして、ガラス基板２１上に走査配線２２と信号配線２４がマトリックス状に形成され、それらの交差位置にＴＦＴ２５が配置され、同時に保護用ＴＦＴ３０が縁部に配設されてアレイ基板２０が製造される。

【００４２】アレイ基板２０が上記のように製造されると、図４に示すように、ドレイン短絡線３９は接地され、ゲート短絡線２９には電池等を用いた直流定電源回路から一定電圧が印加され、これにより、各保護用ＴＦＴ３０のゲート電極３３にオン動作用の電圧が印加され、各保護用ＴＦＴ３０は導通状態とされる。

【００４３】一方、アレイ基板２０と対向して配設される対向基板（図示せず）は、別のガラス基板上に、ＩＴＯ等からなる共通電極を形成して製造される。

【００４４】そして、アレイ基板２０と対向基板の表面（内側）にポリイミド等からなる配向膜を形成し、焼成した後、配向膜の表面にはラビング処理が施される。このラビングを行う際、空気やパイル等の摩擦により非常に多くの静電気が発生する。

【００４５】しかし、アレイ基板２０における各走査配線２２と各信号配線２４は、保護用ＴＦＴ３０とドレイン短絡線３９を通して接地されているため、そこに接続された各ＴＦＴ２５のソース電極２７及びゲート電極２３は同電位となり、静電気による電荷が各走査配線２２や信号配線２４に注入された場合でも、ソース電極２７とゲート電極２３間に高電圧がかかることはなく、静電気によって破壊されやすいソース・ゲート間の絶縁層は確実に保護される。

【００４６】その後、アレイ基板２０は、図示しない対向基板と一定の間隔をおいて重ね合せられ、周囲をシール材（接着剤）でシールして、その内部に液晶が封入され、ガラス基板の縁部を製品形状に切断する等の各種の工程を経て液晶表示装置が製造されるが、図示しない駆動用ＩＣが基板上に実装され各走査配線２２及び信号配線２４に接続されるまで、保護用ＴＦＴ３０は導通状態とされる。

【００４７】このため、各走査配線２２と信号配線２４がドレイン短絡線３９によって短絡された状態は、その後の製造工程でも継続され、製造工程中における作業者との接触や運搬動作等によって静電気が帯電した場合にも、ＴＦＴ２５のソース電極２７及びゲート電極２３は短絡されて、同電位となり、ＴＦＴ２５を保護することができる。

【図面の簡単な説明】

【図１】第一発明の一実施例であって、アクティブマトリックス型液晶表示装置の製造時におけるアレイ基板１０の概略平面図である。

【図２】製品形状に切断された状態の概略平面図である。

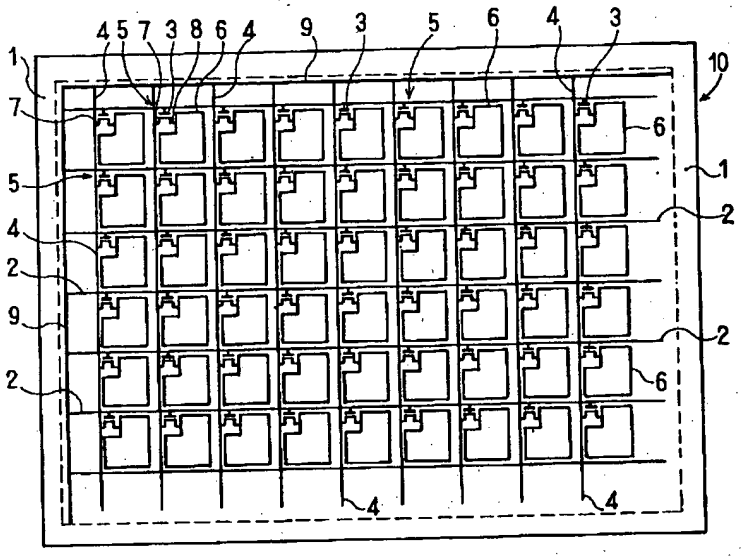
【図３】駆動用ＩＣを実装した状態の概略平面図である。

【図４】第二発明の一実施例であって、アクティブマトリックス型液晶表示装置の製造時におけるアレイ基板１０の概略部分平面図である。

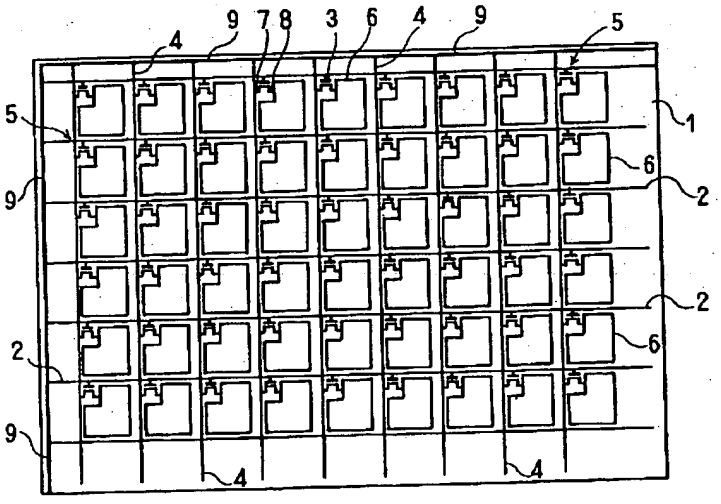
【符号の説明】

１－ガラス基板、２－走査配線、４－信号配線、５－ＴＦＴ、９－短絡線、１０－アレイ基板、１１－駆動用ＩＣ、２９－ゲート短絡線、３０－保護用ＴＦＴ、３９－ドレイン短絡線。

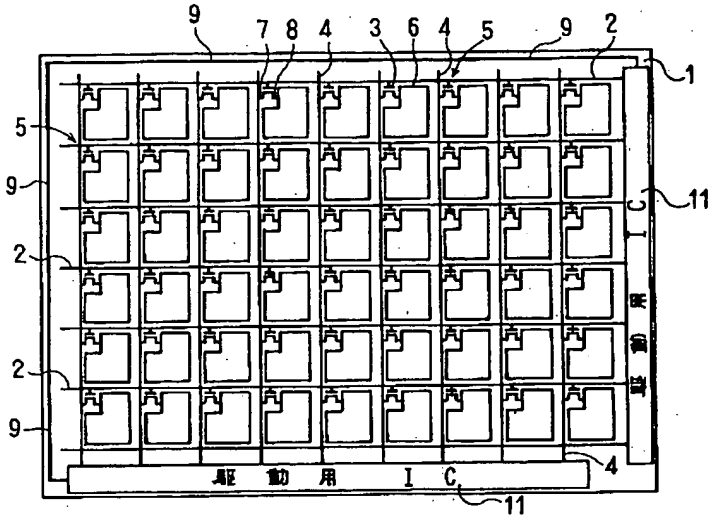
【図１】



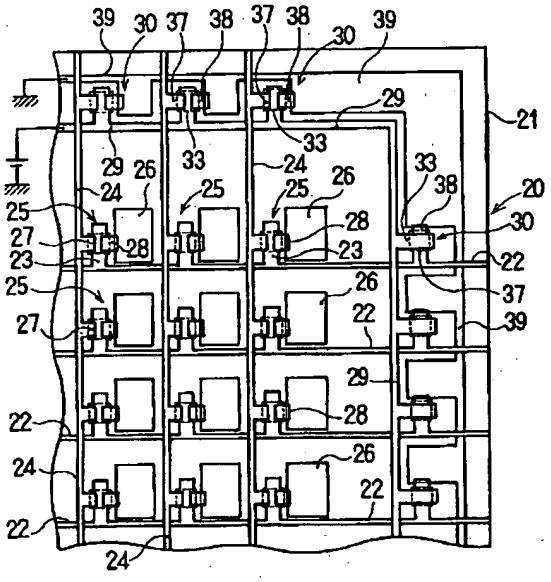
【図２】



【図３】



【図４】



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Inventors: Ryo Sato et al.

[Title of the Invention] PRODUCTION METHOD OF ACTIVE MATRIX TYPE LIQUID CRYSTAL DISPLAY DEVICE

[Abstract]

[Object]

To provide a production method of an active matrix type liquid crystal display device that can satisfactorily protect built-in TFTs from static electric ity and can effectively prevent dielectric breakdown of the TFTs and degradation of their performance.

[Constitution]

A short-circuit line 9 for short-circuiting scanning lines 2 and signal lines 4 is arranged on edge portions of one of glass substrates 1. After a liquid crystal is charged between an array substrate 10 and an opposing substrate, a peripheral portion of the glass substrates is cut into a predetermined shape of a product in such a fashion as to leave the short -circuit

line 9. Driving ICs 11 are thereafter mounted to edge portions of the glass substrate 1, and the scanning lines 2 and the signal lines 4 are connected to the driving ICs 11. The connection portions of the short-circuit line 9 with the scanning lines 2 and the signal lines 4 are then cut off.

[Claims]

[Claim 1]

A production method of an active matrix type liquid crystal display device including scanning lines and signal lines arranged in matrix on one of glass substrates, thin film transistors connected to points of intersection of said scanning lines and said signal lines to constitute an array substrate, an opposing substrate fabricated by forming a common electrode on the other of said glass substrates, an orientation film formed on an upper surface of each of said array substrate and said opposing substrate, and a liquid crystal charged between said array substrate and said opposing substrate after they are bonded to each other in parallel with a spacing between them, said production method characterized by comprising the steps of:

arranging a short-circuit line for short-circuiting said scanning lines and said signal lines on edge portions of said one glass substrate;

cutting a peripheral portion of said glass substrates into a predetermined shape of a product in such a fashion as

to leave said short-circuit line after said liquid crystal is charged between said array substrate and said opposing substrate;

mounting driving integrated circuits onto edge portions of said glass substrate;

connecting said scanning lines and said signal lines to said driving integrated circuits; and

cutting off the connection portions of said short-circuit line with said scanning lines and said signal lines.

[Claim 2]

A production method of an active matrix type liquid crystal display device including scanning lines and signal lines arranged in matrix on one of glass substrates, thin film transistors connected to points of intersection of said scanning lines and said signal lines to constitute an array substrate, an opposing substrate fabricated by forming a common electrode on the other of said glass substrates, an orientation film formed on an upper surface of each of said array substrate and said opposing substrate, and a liquid crystal charged between said array substrate and said opposing substrate after they are bonded to each other in parallel with a spacing between them, said production method characterized by comprising the steps of:

arranging a large number of protective thin film transistors on edge portions of said one glass substrate in such a fashion as to correspond to said scanning lines and to

said signal lines;

arranging a drain short-circuit line for short-circuiting drain electrodes of said protective thin film transistors along edge portions of said glass substrate;

arranging a gate short-circuit line for short-circuiting gate electrodes of said protective thin film transistors along edge portions of said glass substrate;

grounding said drain short-circuit line during a subsequent production step; and

applying a predetermined voltage to said gate short-circuit line during a subsequent production step to bring said protective thin film transistors into a conductive state.

[Detailed Description of the Invention]

[0001]

[Industrial Field of Application]

This invention relates to a production method of an active matrix type liquid crystal display device for displaying images by arranging a thin film transistor (hereinafter abbreviated as "TFT") for each pixel and causing it to conduct a switching operation.

[0002]

[Prior Art]

The active matrix type liquid crystal display device of this kind basically has the following construction. Scanning

lines and signal lines are arranged in matrix on one of glass substrates and TFTs and pixel electrodes ar e arranged at points of intersection of these lines to constitute an array substrate. A common electrode is formed on the other of the glass substrates to constitute an opposing substrate. An orientation film is formed on an upper surface of each of the array substrate and the opposing substrate. The array substrate and the opposing substrate are bonded to each other in parallel with spacing between them, and a liquid crystal is charged and sealed between the array substrate and the opposing electrode.

[0003]

In the production process of such a liquid crystal display device, large quantities of static electricity develop due to air streams inside a production chamber, friction of clothes of operators or rubbing treatment of orientation films or the like. The TFTs built in the liquid crystal display device are extremely susceptible to static electricity of this kind. Particularly when large quantities of static electricity develop and the charge of this static electricity is applied to the scanning lines and to the signal lines, a high voltage occurs between each scanning line and each signal line. Consequently, dielectric breakdown occurs inside the TFTs connected to these lines and performance of the TFTs gets deteriorated either partially or wholly.

[0004]

To cope with this problem, it has been customary to employ the following construction. A short-circuit line is arranged on a peripheral portion of an array substrate during its production and all of scanning lines and signal lines are connected to the short-circuit line so as to let static electricity developing at the time of rubbing treatment of an orientation film, etc, flow through the short-circuit line and to protect the TFTs.

[0005]

However, it is not possible to carry out a disconnection/short-circuit test, a probe test, and so forth, of the TFTs or the like in the production steps during the production of such an array substrate while the scanning line and the signal line are kept connected to the short-circuit line. Therefore, after the liquid crystal panel is formed by bonding the array substrate and the opposing substrate to each other and sealing the liquid crystal after the rubbing treatment, each scanning line and each signal line are cut off from the short-circuit line.

[0006]

Consequently, the TFT is left unprotected from static electricity until the driving ICs are connected to the scanning lines and to the signal lines after these lines are cut off from the short-circuit line. When static electricity develops due to contact with human bodies and at the time of transportation

of the product during the production process in the interim, the problems of dielectric breakdown of the TFTs and degradation of their performance described above occur.

[0007]

[Problems that the Invention is to Solve]

To prevent degradation of performance of the TFTs and their dielectric breakdown inside the liquid crystal panel during the production, various counter-measures against static electricity such as a technology that covers the entire surface of the array substrate with an insulating film (JP-A-64-32234) and a technology that arranges a dummy electrode at a peripheral edge portion of the array substrate and collects the charge of static electricity to the dummy electrode to protect the inner TFT (JP-A-64-59320 and JP-A-64-59321) have been proposed in the past.

[0008]

However, any of these technologies have not been entirely satisfactory to sufficiently protect the TFTs from static electricity, and the problem of the drop of the production yi eld has remained yet unsolved.

[0009]

To solve the problems described above, it is an object of the invention to provide a production method of an active matrix type liquid crystal display device that can satisfactorily protect built-in TFTs from static electricity

and can effectively prevent dielectric breakdown of the TFTs and degradation of their performance.

[0010]

[Means for Solving the Problems]

In a production method of an active matrix type liquid crystal display device including scanning lines and signal lines arranged in matrix on one of glass substrates, thin film transistors connected to points of intersection of the scanning lines and the signal lines to constitute an array substrate, an opposing substrate fabricated by forming a common elec trode on the other of the glass substrates, an orientation film formed on an upper surface of each of the array substrate and the opposing substrate and a liquid crystal charged between the array substrate and the opposing substrate after they are bonded t o each other in parallel with a spacing between them, a production method according to a first invention comprises the steps of arranging a short-circuit line for short-circuiting the scanning lines and the signal lines on edge portions of the one glass substrate; cutting a peripheral portion of the glass substrates into a predetermined shape of a product in such a fashion as to leave the short-circuit line after the liquid crystal is charged between the array substrate and the opposing substrate; mounting driving integrated circuits onto edge portions of the glass substrate; connecting the scanning lines and the signal lines to the driving integrated circuits; and

cutting off the connection portions of the short-circuit line with the scanning lines and the signal lines.

[0011]

In a production method of an active matrix type liquid crystal display device including scanning lines and signal lines arranged in matrix on one of glass substrates, thin film transistors connected to points of intersection of the s canning lines and the signal lines to constitute an array substrate, an opposing substrate fabricated by forming a common electrode on the other of the glass substrates, an orientation film formed on an upper surface of each of the array substrate and the opposing substrate and a liquid crystal charged between the array substrate and the opposing substrate after they are bonded to each other in parallel with a spacing between them, a production method according to a second invention comprises the steps of arranging a large number of protective thin film transistors on edge portions of the one glass substrate in such a fashion as to correspond to the scanning lines and the signal lines; arranging a drain short-circuit line for short-circuiting drain electrodes of the protective thin film transistors along edge portions of the glass substrate; arranging a gate short-circuit line for short-circuiting gate electrodes of the protective thin film transistors along edge portions of the glass substrate; grounding the drain short-circuit line during a subsequent production step; and applying a predetermined voltage to the

gate short-circuit line to bring the protective thin film transistors into a conductive state.

[0012]

[Mode of Operation and Advantages of the Invention]

In the production method according to the first invention, the short-circuit line short-circuits each scanning line and each signal line during the process steps of the active matrix type liquid crystal display device such as in the steps of rubbin g treatment and sealing of the liquid crystal and in the subsequent step of cutting the peripheral edge portion of the glass substrates into the shape of the product until each of the scanning line and the signal line is connected to the driving IC. Therefore, the source electrode and the gate electrode of each TFT connected to these lines are short-circuited and attain the same potential. Even when the charge resulting from static electricity is injected to each of the scanning line and the signal line, a high voltage is not applied across the source electrode and the gate electrode of the TFT, and an insulating layer between the source and the gate that is otherwise likely to undergo dielectric breakdown due to static electricity can be reliably protected.

[0013]

After the driving ICs are mounted to the edge portions of the glass substrates and are connected to the scanning lines and to the signal lines, the connection portion of the

short-circuit line with the scanning line and the signal line is cut off. Therefore, the scanning line and the signal line, that have been released in the prior art devices when the short-circuit line is cut off from the scanning line and the signal line, are not released. In other words, the period in which the lines are released from cut-off of the short circuit line to connection of the driving IC to the scanning line and to the signal line does not exist, and the TFTs can be effectively protected from static electricity throughout the entire production process.

[0014]

In the production method according to the second invention, a large number of protective thin film transistors are arranged on the edge portions of the glass substrate during the production process of the array substrate in such a fashion as to correspo nd to the scanning lines and to the signal lines, the drain short-circuit line for short-circuiting the drain electrodes of the protective thin film transistors is arranged along the edge portions of the glass substrate, and the gate short -circuit line for short-circuiting the gate electrodes of the protective thin film transistors is arranged along the edge portions of the glass substrate. The drain short -circuit line is grounded in the subsequent steps of rubbing treatment and sealing of the liquid crystal, and a predetermined voltage is applied to the gate short-circuit line to bring the protective thin film

transistors into the conductive state.

[0015]

Therefore, each of the scanning lines and the signal lines is always kept grounded through the protective TFT and through the drain short-circuit line during the production process, and the source electrode and the gate electrode of each TFT are short-circuited and attain the same potential. Even when the charge of static electricity is injected into each scanning line and each signal line, a high voltage is not applied across the source electrode and the gate electrode of each TFT, and the insulating layer between the source and the gate that is otherwise likely to undergo dielectric breakdown due to static electricity can be reliably protected.

[0016]

[Embodiment]

Preferred embodiments of the invention will be hereinafter explained with reference to the accompanying drawings.

[0017]

Fig. 1 to Fig. 3 show an embodiment according to a first invention, wherein Fig. 1 is a schematic plan view of an array substrate 10 when an active matrix type liquid crystal display device is produced.

[0018]

When the array substrate 10 is produced, a large number

of scanning lines 2 are first formed on a glass substra te 1 in parallel with one another with predetermined spacing among them. Gate electrodes 3 of a large number of TFTs 5 are connected respectively to the scanning lines 2 at positions where the TFTs 5 are to be arranged. The scanning line 2 and the gate electrode 3 are formed of a metal such as chromium by a method such as sputtering and photolithography.

[0019]

In this instance, an L-shaped short-circuit line 9 is formed of a metal such as chromium at edge portions of the glass substrate such as at the upper end portion and at the left edge portion in Fig. 1. A left end portion of each scanning line 2 is connected to this short-circuit line 9.

[0020]

Next, a gate insulating film is formed on the gate electrode 3 of each TFT 5 and an active layer and a doping layer are formed in an island form on the gate insulating film.

[0021]

Next, a pixel electrode 6 is formed of a metal such as ITO on the gate insulating film by a method such as sputtering and photolithography. A large number of signal lines 4 of a metal such as molybdenum or aluminum are formed in parallel with one another and with predetermined spacing among them in a direction crossing at a right angle the scanning lines 2. A source electrode 7 of each TFT 5 is formed of a similar metal

and by a similar method and is connected to each signal line 4. A drain electrode 8 is connected to the pixel electrode 6. The upper end of each of these signal lines 4 is connected to the short-circuit line 9 arranged at the upper edge position as shown in Fig. 1.

[0022]

The scanning lines 2 and the signal lines 4 are formed in matrix on the glass substrate 1 in the manner described above, and the TFTs 5 are arranged at their points of intersection to complete the array substrate 10.

[0023]

On the other hand, an opposing substrate (not shown in the drawings) that is to be so arranged as to oppose the array substrate 10 is fabricated when a common electrode of ITO , etc., is formed on another glass substrate.

[0024]

An orientation film made of polyimide, or t he like, is formed on the surface (inner surface) of each of the array substrate 10 and the opposing substrate. After baked, the surface of the orientation film is subjected to rubbing treatment. Extremely large quantities of static electricity develop d ue to friction of air and pile and so on when this rubbing treatment is carried out. Since the short-circuit line 9 short-circuits each scanning line 2 and each signal line 4 on the array substrate 10, however, the source electrode 7 of each TFT 5 and its gate

electrode 3 which are connected to these lines are short-circuited and attain the same potential. In consequence, even when the charge resulting from static electricity is injected to each scanning line 2 and each signal line 4, a high voltage is not applied between the source electrode 7 and the gate electrode 3, and the insulating layer between the source and the gate that is otherwise likely to undergo breakdown due to static electricity can be reliably protected.

[0025]

Next, the array substrate 10 and the opposing electrode are put one upon another in such a fashion as to let the orientation films oppose each other and keep a predetermined spacing between them. A sealant (adhesive) is applied to the periphery of the resulting assembly with the exception of a portion that is to operate as an injection port. After the sealant is baked, liquid crystal is injected from the injection port between the substrates and the injection port is then sealed.

[0026]

The peripheral portion of the glass substrates of the array substrate 10 and the opposing substrate is cut off in a predetermined dimension into a product shape. In this case, the edge portion is cut in such a fashion as to leave the short-circuit line 9 on the glass substrate 1 as shown in Fig. 2. Therefore, the short-circuit state of the scanning line 2 and the signal line 4 by the short-circuit line 9 is thereafter

kept as such. Even when static electricity is charged due to contact with operators during the production process or due to transportation or the like, the source electrode 7 and the gate electrode 3 of the TFT 5 are short-circuited and attain the same potential with the result that the TFT 5 can be protected similarly as described above.

[0027]

Incidentally, one short-circuit line 9 short-circuits each scanning line 2 and each signal line 4 in the explanation given above. However, it is possible to cut off the short-circuit line connected to each scanning line 2 (a vertical portion in the drawing) from the short-circuit line connected to each signal line 4 (a horizontal portion) and to insert a high resistance between them. In this way, it becomes possible to test performance of the TFTs 5 by utilizing the short-circuit line while the TFTs 5 are protected from static electricity.

[0028]

This liquid crystal display device is of a so-called "COG" type in which the driving ICs are directly mounted to the glass substrate 1. The spaces for mounting the driving ICs are formed at the right edge portion of the glass substrate 1 and its lower edge portion as shown in Fig. 2.

[0029]

Here, the driving ICs 11 are mounted to the spaces of the right edge portion of the glass substrate 1 and its lower

edge portion as shown in Fig. 3 in such a fashion that each terminal is connected to the extension portions of the scanning line 2 and the signal line 4. The short-circuit line 9 is connected to a GND terminal of the driving IC 11.

[0030]

After the driving ICs 11 are mounted, the connection portion of each scanning line 2 and each signal li ne 4 with the short-circuit line 9 is cut off by using a laser cutter, or the like as shown in Fig. 3

[0031]

After the driving ICs 11 are mounted to the edge portions of the glass substrate 1 and are connected to the scanning line 2 and to the signal line 4, the connection portion of the short-circuit line 9 with the scanning line 2 and the signal line 4 is cut off as described above. In the prior art devices, the short-circuit line is cut off and removed simultaneously with cutting of the edge portion of the glass substrates, thereby releasing the scanning line from the signal line. In the invention, however, the scanning line and the signal line are not released from each other and the TFTs 5 can be effectively protected from static electricity throughout the production process as a whole.

[0032]

The short-circuit line 9 remains connected to the GND terminal of the driving ICs 11 under the product state.

Therefore, a conductor line that is grounded to the earth is disposed at the edge of the liquid crystal display device and is helpful for the protection of the product from static electricity.

[0033]

Fig. 4 shows an embodiment according to a second embodiment of the invention, and is a schematic plan view of an array substrate 20 during production.

[0034]

To produce this array substrate 20, a large number of scanning lines 22 are formed on a glass substrate 21 with predetermined spacing among them. Gate electrodes 23 of a large number of TFTs 25 are connected respectively to the scanning lines 22 at positions at which the TFTs 25 are to be arranged. The scanning line 22 and the gate electrode 23 are formed of a metal such as chromium by use of a method such as sputtering and photolithography.

[0035]

At the same time, a gate shot-circuit line 29 is formed of a metal such as chromium at edge portions of the glass substrate 21 such as its upper edge portion and a right edge portion in Fig. 4, and a gate electrode 33 of each protective TFT 30 to be later described is formed in such a fashion as to b e connected to the gate short-circuit line 29. The protective TFTs 30 are arranged along the upper edge portion and the right edge portion

of the glass substrate 20 in such a fashion as to correspond to the scanning lines 22 and to signal lines 24 to be later described.

[0036]

Next, a gate insulating film is formed on the gate electrode 23 of each TFT 25 and on the gate electrode 33 of each protective TFT 30, and an active layer and a doping layer are formed in an island form on the gate insulating film.

[0037]

A pixel electrode 26 is formed on the gate insulating film by use of a metal such as ITO and a method such as sputtering and photolithography and at the same time, a drain short -circuit line 39 is formed by use of the same metal and the same meth od along the upper edge portion and the right edge portion of the glass substrate 1.

[0038]

Next, a large number of signal lines 24 are formed by use of a metal such as molybdenum, aluminum , and the same method with predetermined spacing among them in a direction crossing at a right angle the scanning lines 22.

[0039]

A source electrode 27 of each TFT 25 is then formed by use of the same metal and the same method and is connected to each signal line 24. Each drain electrode 28 is formed and connected to the pixel electrode 26 and at the same time, a

drain electrode 38 of each protective TFT 30 is formed and connected to a drain short-circuit line 39. Furthermore, a source electrode 37 of each protective TFT 30 is formed and connected to each signal line 24.

[0040]

Incidentally, because the protective TFT 30 is formed on the glass substrate 21 simultaneously with the formation of the TFT 25, the protective TFT 30 arranged at the right edge portion in Fig. 4 may be of a staggered type in which its gate side and its source/drain side are oppositely formed when the protective TFT 30 arranged at the upper edge portion is of an inverse staggered type.

[0041]

The scanning lines 22 and the signal lines 24 are formed on the glass substrate 21 in the matrix fo rm in the manner described above, and the TFTs 25 are arranged at the points of their intersection. At the same time, the protective TFTs 30 are formed at the edge portions, thereby completing the array substrate 20.

[0042]

After the array substrate 20 is produced as described above, the drain short-circuit line 39 is grounded as shown in Fig. 4. A predetermined voltage is applied from a D. C. constant power circuit using a battery, etc, to the gate short-circuit line 29. Consequently, an ON operation voltage

is applied to the gate electrode 33 of each protective TFT 30 and each protective TFT 30 becomes thus conductive.

[0043]

On the other hand, an opposing substrate (not shown) to be so arranged as to oppose the array substrate 20 is completed when a common electrode of ITO, etc, is formed on another glass substrate.

[0044]

An orientation film made of polyimide, or the like, is formed on the surface (inner surface) of each of the array substrate 20 and the opposing substrate. After baked, the surface of the orientation film is subjected to rubbing treatment. Extremely large quantities of static electricity develop due to friction of air and pile and the like when this rubbing treatment is carried out.

[0045]

Since each scanning line 22 and each signal line 24 on the array substrate 20 are grounded through the protective TFT 30 and through the drain short-circuit line 39, however, the source electrode 27 of each TFT 25 and its gate electrode 23 attain the same potential. In consequence, even whe n the charge resulting from static electricity is injected to each scanning line 22 and to each signal line 24, a high voltage is not applied between the source electrode 27 and the gate electrode 23, and the insulating layer between the source and the gat e that is

otherwise likely to undergo breakdown due to static electricity can be reliably protected.

[0046]

Next, the array substrate 20 and the unillustrated opposing electrode are put one upon another in such a fashion as to keep a predetermined spacing between them. A sealant (adhesive) is applied to the periphery of the resulting assembly and a liquid crystal is injected. The edge portions of the glass substrates are cut off, and the liquid crystal display device is thus produced. Driving ICs, not shown, are mounted to the substrate and are connected to each scanning line 22 and to each signal line 24. In the interim, each protective TFT 30 is kept conductive.

[0047]

Therefore, the short-circuit state of each scanning line 22 and each signal line 24 by the drain short-circuit line 39 is kept as such during the subsequent production process. Even when static electricity is charged due to contact with operators during the production process or due to transportation, the source electrode 27 and the gate electrode 23 of the TFT 25 are short-circuited and attain the same potential with the result that the TFT 25 can be protected.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a schematic plan view of an array substrate 10 during a production process of an active matrix type liquid crystal display device according to an embodiment of a first invention.

[Fig. 2]

Fig. 2 is a schematic plan view under a state where the array substrate is cut into a shape of a product.

[Fig. 3]

Fig. 3 is a schematic plan view showing a state where driving ICs are mounted.

[Fig. 4]

Fig. 4 is a partial schematic plan view of an array substrate 10 during production of an active matrix type liquid crystal display device according to an embodiment of a second invention.

[Description of Reference Numerals]

1: glass substrate

2: scanning line

4: signal line

5: TFT

9: short-circuit line

10: array substrate

11: driving IC

29: gate short-circuit line

30: protective TFT

39: drain short-circuit line